Design and modeling of a digital controller for SMPS

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Abstract: In many different applications, where battery operated devices are involved, dc-dc converters with high efficiency over the whole range of their load values are required. In particular, optimization of the efficiency of these converters when the load current is low, i.e. at light load, has become one of the most challenging issues in designing dc-dc converters. In multi-mode dc-dc converters the controller implements different control strategies according to the output current demand, in order to keep the efficiency as high as possible over the whole range of load values. In this context, control of switched mode power supplies (SMPS) has been traditionally achieved through analog means with dedicated integrated circuits (ICs). However, as power systems are becoming increasingly complex, the classical concept of control has gradually evolved into the more general problem of power management, demanding functionalities that are hardly achievable in analog controllers. The high flexibility offered by digital controllers and their capability to implement sophisticated control strategies, together with the programmability of controller parameters, make digital control very attractive as an option for improving the features of multimode dc-dc converters. Moreover, although digital control in power electronics is potentially able to meet the aforementioned requirements of modern power supply systems and electronic equipments, analog control ICs for power converters are still dominating the market. Indeed, digital control for SMPS lacks of a strong and well established know-how as analog control does and, therefore, is less accessible to designers.

Keywords: Field-programmable gate arrays (FPGA), digital signal processor (DSP), very high speed integrated circuit hardware description language (VHDL).

1. Introduction

Control of SMPS intended for consumer market has been traditionally achieved by analog means. Nowadays, analog control ICs are available at low price and for a variety of power applications and converter topologies. These controllers typically integrate one or more error amplifiers, modulation circuitry, a temperature-compensated voltage reference, overvoltage/overcurrent protections as well as soft-start, standby and automatic shutdown features. Depending on the power rating, gate drivers and power switches may be integrated or left as off-chip components. Off-chip passive circuitry is used to program the controller behavior, define the shape of the compensator transfer function and provide feedback and sensing interfaces between the chip and the power converter. With the rapid development and diffusion of battery operated portable devices, requirements such as power quality, high efficiency, tight output voltage regulation, area optimization and minimization of external components are demanded. Many analog solutions have been developed for applications such as mobile phones, portable instruments, portable hard disk drivers etc. where the efficiency is kept as high as possible over a wide range of output currents by the use of dedicated control strategies that involve complex analog circuitry to properly manage the operations of the converter. Nevertheless, the implementations of sophisticated controllers by the use of analog solutions have come to limitations due to the hardware involved. To further
improve converter performances, therefore, digital solutions have become attractive in this field.

Digital control for SMPS has started to gain popularity. The main advantages deriving from the implementation of a digital loop in dc-dc converter systems are represented by the high degree of programmability and computational power, the reduced need for external passive components and the consequent decreased sensitivity to tolerances and other sources of parametric variations, the possibility to implement complex control strategies as well as to easily switch through different modes of operation, targeting for highest efficiency or optimized dynamic performances. System monitoring functions are of extreme importance for high-reliability applications and their implementation strongly points to digital solutions able to collect and process environmental data. Self-tuning, also known as auto tuning functions, allow a digital compensator to adapt its parameters to the specific power plant under control, eliminating the need for manual design or calibration and enhancing controller modularity and versatility [7].

In general, compared to the existent analog solutions, digital controlled SMPS would not able to obtain the same features, in terms of output voltage regulation, if additional functionalities and more complex control strategies were not involved, functionalities that justify the cost and the effort to be developed. In fact, digital control wins, where the algorithms of the operation is too complex for analog implementations. No analog controller exhibits the same degree of programmability and versatility as a digital controller does. Compensator parameters can be stored in a nonvolatile memory and loaded in a programmable controller at system power-on. This way, different sets of pre-calculated parameters can be run for many environmental conditions on the same control hardware. More evolved tuning algorithms literally perform an automatic design of the compensator parameters through a number of online measurements and post-processing operations [6].

The power converter is modeled by the digital control is described in very high speed integrated circuit hardware description language (VHDL) by using Active-HDL, and the complete system is simulated in MATLAB/Simulink environment [3]. The pulse width modulation (PWM) has been widely used in power converter control and most high power level converters operate at high switching frequencies. The developments of high-frequency PWM generator architecture for power converter are control by FPGA’s [13].

2. Materials and methods

The quality of the electrical current is a major concern in recent time. The power electronic equipments induce harmonic disturbances in the power distribution systems. They typically draw non-sinusoidal currents from the utility, causing interference with adjacent sensitive loads and limit the utilization of the available electrical supply. The quality of the electrical current thus becomes a significant concern for the distributors of energy and their customers. This section of the paper deals with some of the digital control techniques, which handle such types of problem with merits and better utility.

The different converters are taken into account and the controllers are now capable to operate all converters efficiently. The converters are used for different power supplies to reduce the ripple contents and improve power quality as per requirements. The software are used for digital control of switching for smoothing and customised as user friendly.

2.1 FPGA-based dc-dc converter

The block diagram of boost converter consists of PWM generator, optoisolator, driver, MOSFET switch, Filter as shown in fig.1.

![Fig 1. Block diagram of Boost converter](image)
tooth waveform and the reference voltage signal. Sawtooth wave generator, a comparator and other auxiliary circuits are integrated on the chip. The function of optoisolator (6N137 or 4506) is to isolate the control circuit from power circuit. PWM signal from TL494IC is not directly fed to the power circuit. In order to protect the PWM signal it is essential to provide isolation circuit between power circuit and control circuit. A MOSFET drive circuit (IR2110) is designed to connect the gate directly to a voltage bus with no intervening resistance other than the impedance of the drive circuit switch. Gate driver acts as a high-power buffer stage between the PWM output of the control device and gates of the primary power switching MOSFET. MOSFET switch (IRF250) is used as a switching device in the boost converter circuit. The PWM signal from the driver IC is fed to the gate of the switch.

Fig. 2. Practical set up for digital controlled dc-dc converter

The drain of the switch is connected to the primary of the isolation transformer. This switched voltage signal undergoes rectification in the filter circuit. Finally rectified pure DC signal is seen at the output terminal. The filter capacitor gives the ripple eliminated pure DC to the output. The Spartan-6E Starter Kit board prominently features a 4-line by 20-character liquid crystal display (LCD) The FPGA controls the LCD via the 8-bit data interface as shown in fig. 2. Once mastered, the LCD is a practical way to display a variety of information using standard ASCII and custom characters. However, these displays are not fast. Scrolling the display at half-second intervals tests the practical limit for clarity. Compared with the 20 MHz clock available on the board, the display is slow. The controller has three internal memory regions, each with a specific purpose. The display must be initialized before accessing any of these memory regions. The Display Data RAM (DD RAM) stores the character code to be displayed on the screen. Most applications interact primarily with DD RAM. The character code stored in a DD RAM location references a specific character bitmap stored either in the predefined CG ROM character set or in the user-defined CG RAM character set.

2.2 FPGA-based real-time emulation

A device-level real-time model implemented in a field programmable gate array (FPGA), for a six-pulse IGBT-based VSC drive, which takes into account the precise switching times albeit based on linear device characteristics. The numerical models utilize finite-element methods to model the carrier diffusion in the device, resulting in a very detailed, although computationally expensive and model [12].

Fig. 3. Circuit to measure IGBT characteristics

The measurements are based on hard switching of the IGBT. The measured IGBT characteristics are used to develop the three-level VSC model. The Powerex CM50DU-24F IGBT module consists of two IGBTs and two anti parallel diodes rated at 1200 V and 50 A. The test circuit shown in Fig. 3 utilizes this module to measure the IGBT characteristics.

A digital multi-mode controller structure is presented for high efficiency low cost and low power dc-dc converter. Moreover, decision criteria for selecting among the control strategies are proposed and tested in an FPGA-based experimental prototype. Finally, the development of a discrete time large-signals model of the converter power stage, particularly suited to predict converter behavior when
transitioning between the different controls strategies, provides a useful tool for designing SMPS according to the above mentioned decision criteria and highlights the main design issues in the power management.

2.3 High-frequency PWM implementation:

In many applications it is desirable to control a power converter using a microcontroller or a digital signal processor (DSP) for the implementation of sophisticated control schemes, such as fuzzy control. The block diagram of such a configuration is depicted in Fig. 4. A set of sensors, used to measure the power converter signals of interest, such as the output current or voltage, output frequency, etc., are interfaced through an analog to digital (A/D) converter to a microcontroller or DSP unit [13].

![Fig. 4 General block diagram for digital power converter control](image)

The measured parameters are input to a digital controller in order to adjust the duty cycle of the PWM signals, which further control the power converter operation, according to the desired control laws, such as fuzzy logic control, PID control, neural networks control, etc. For reduction of the total system cost, it is necessary to integrate all operations in a single IC.

![Fig. 5 The PWM generator architecture](image)

Each PWM signal is usually generated using an on-chip PWM generator and built according to the general block diagram shown in Fig. 5. An N-bit value, corresponding to the desired duty cycle value is compared with the value of an N-bit counter running with clock frequency $f_{clock}$. The comparator output is used to trigger a toggle register, producing a PWM output signal with adjustable duty cycle. This configuration has the disadvantage that the resulting signal frequency, which defines the power converter switching frequency, limited by the microcontroller or DSP unit clock frequency. Using an N-bit resolution, resulting in $2^N$ different duty cycle states, the clock frequency, $f_{clock}$, is related to the PWM output wave frequency, $f_{PWM}$, as follows:

$$f_{PWM} = \frac{f_{clock}}{2^N}$$  \hspace{1cm} (1)

Assuming that an 8-bit resolution is desired, then the required clock speed for a 100 kHz, PWM signal is 25.6 MHz, while for a 500 kHz PWM frequency output the required clock frequency is 128 MHz, which cannot be supported by a microcontroller or DSP unit.

3. Module and results of PWM generator

Due to the advances of solid state power devices and microprocessors, switching power converters are used. The energy that a switching power converter delivers to a load is controlled by pulse width modulated (PWM) signals applied to the gates of the power transistors. PWM signals are pulse trains with fixed frequency and magnitude and variable pulse width. There is one pulse of fixed magnitude in every PWM period. However, the width of the pulses changes from pulse to pulse according to a modulating signal. When a PWM signal is applied to the gate of a power transistor, it undergoes turn on and turns off intervals of the transistor to change from one PWM period to another according to the same modulating signal. The frequency of a PWM signal must be much higher than that of the modulating signal, the fundamental frequency, such that the energy delivered to the load depends mostly on the modulating signal.

3.1 MATLAB module for PWM generator

This section of the paper is deal with MATLAB module and waveforms of PWM generator. Fig. 6 shows the MATLAB module, first of all the designer need to create a system model using simulink editor, obtaining a block diagram model of the
dynamic system described by a set of algebraic, differential and/or difference equations.

![Fig. 6 MATLAB module for PWM generator](image)

After creating the model by using simulink libraries components, the designer can run simulation, fixing a specified start and stop time. The interactive graphical environment and the customizable/specialized set of available libraries make simulink a versatile and powerful instrument for researchers and engineers. Fig 7 shows the PWM waveform generation on MATLAB module.

### 3.2 FPGA Module for PWM generator

The basic VHDL module is an introduction to the VHSIC hardware description language and its fundamental concepts. VHDL is a language specifically developed to describe digital electronic hardware and its attributes. VHDL is a flexible language and can be applied to many different design situations. This language has several key advantages, including technology independence and a standard language for communication. The module describes many of the advantages of using VHDL and a short history of the language. This section of the paper deals with FPGA Module for PWM generator [14].

![Fig. 7 Simulation results for MATLAB module](image)

![Fig. 8. FPGA Module for PWM generator](image)

A FPGA is an integrated circuit designed to be configured by the customer or designer after manufacturing. The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an ASIC. FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality, partial re-configuration of the portion of the design and the low non-recurring engineering costs relative to an ASIC design offer advantages for many applications. FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together" somewhat like many logic gates that can be inter-wired in (many) different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

Fig 8 shows a FPGA module for PWM generator. As FPGA is a very convenient tool, with a combined hardware/software system, the designer can partition tasks based on the requirements. Algorithmically complex tasks can be handled in software, while computationally intensive ones can be handled in hardware. Furthermore, the flexibility
3.3 Single-Phase PWM Inverter

Fig. 9 and 10 illustrates insulated gate bipolar transistor (IGBT)/diode block in voltage-sourced converters & also harmonic analysis of PWM waveforms using the fast Fourier transform (FFT) tool. The system consists of two circuits of single-phase PWM voltage-sourced converters (VSC), namely half-bridge inverter and full-bridge inverter. The inverters are built with the IGBT/diode block which is the basic building block of all VSCs. The IGBT/diode block is a simplified model of an IGBT/diode pair where the forward voltages of the forced-commutated device and diode are ignored.

The two circuits use the same DC voltage (Vdc = 400V), carrier frequency and modulation index (m = 0.8). In order to allow further signal processing, signals displayed on the two scope blocks are stored in two variables names. Simulation presents two waveforms of load current and voltage generated by the PWM inverter shown in fig 11 and 12.

Fig. 11 shows the half-bridge inverter generates a bipolar voltage (-200V or +200V). Harmonics occur around the carrier frequency with a maximum of 103% at 1080 Hz. Fig. 12 shows the full-bridge inverter generates a monopolar voltage varying between 0 and +400V for one half cycle and then between 0 and -400V for the next half cycle. For the same DC voltage and modulation index, the fundamental component magnitude is twice the value obtained with the half-bridge. Harmonics generated by the full-bridge are lower and they appear at double of the carrier frequency. As a result, the current obtained with the full-bridge is smoother.

In "FFT Analysis" to display the 0 - 5000 Hz frequency spectrum of signals saved in the three structures. The FFT will be performed on a 2-cycle window starting at t = 0.1 - 2/60. The fundamental component of Vinverter is obtained on window. Magnitude of the fundamental component of the inverter voltage with the theoretical values given in the circuit is compared. Also compare the harmonic contents of the inverter voltage. There are two spectral estimation techniques based on the Fourier transform
based on the indirect approach and the direct approach via FFT operation. The following equations (2, 3) are used to calculate the harmonic estimation using Prony method.

\[ y[n] = \sum_{k=1}^{N} A_k e^{j(\omega_k n + \phi_k)T_p + \phi_k} \]

where \( n = 1, 2, ..., N \), \( T_p \) - sampling period, \( A_k \) - amplitude, \( a_k \) - damping factor, \( \omega_k \) - angular velocity, \( \phi_k \) - initial phase. The discrete-time function may be concisely expressed in the form

\[ y[n] = \sum_{k=1}^{N} h_k Z_k^{n-1} \]

Where \( h_k = A_k e^{j\omega_k} \), \( Z_k = e^{j(\omega_k + \phi_k)T_p} \)

FFT analysis on the signal "I load" gives the THD of load current is 7.24\% for the half-bridge inverter as compared to only 2.01\% for the full-bridge inverter as shown in fig. 13 and 14.

There are several industrial applications which may allow a harmonic content of 5\% of its fundamental component of input voltage when inverters are used. Actually, the inverter output voltage may have harmonic content much higher than 5\% of its fundamental component. In order to bring this harmonic content much reasonable limit of 5\% and the frequency harmonics method can be reduced by a low-size filter. For the attenuation of low-frequency harmonics, however, the size of filter components increases. This makes the filter circuit costly, bulky and weightily and in addition, the transient response of the system becomes sluggish. This shows that the lower order harmonics from the inverter output voltage should be reduced by some means other than the filter. Subsequent to this, high frequency component from this voltage can easily be attenuated by a low-size, low-cost filter [15].

4. Harmonic measurement of SMPS for television

A SMPS for television typically consists of a power transformer, secondary side rectifier diodes, a switching semiconductor device, a control IC, and peripheral circuits. Besides its basic function of supplying power to the load on the secondary side, an SMPS may have to perform other, special functions, depending on the system. For example, an SMPS for a colour television receiver must minimize the effect of switching noise on the screen and reduce power consumption in standby. If the level of integration of the switching circuitry is not high enough, then additional, separate circuits will be required to accommodate all functions. Harmonics are measured for colour television by fluke 41b - power harmonics analyser at SSBTCOET, Bambhori, Jalgaon. Fig 15
shows analog type SMPS is used in television and found current up to 11th harmonic.

Table 1. Current harmonic measurement

<table>
<thead>
<tr>
<th>Harmonics</th>
<th>Freq.</th>
<th>I Mag</th>
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Table 1 shows the measured harmonics in SMPS. The total harmonic distortion for fundamental current is 123.85 and for rms current are 77.80.

Fig. 16 shows the harmonics present in SMPS of television. Above techniques may be used to reduce the harmonics. The most frequently used power circuits in household appliances are the flyback converter and the forward converter, both of which use the pulse width modulation (PWM) control method for fixed frequency switching. However, a general purpose PWM based SMPS cannot be used for a monitor or colour TV, because the SMPS’s switching noise would seriously affect the display quality. The switching noise would appear in the form of picture noise. To significantly reduce the effect of switching noise on the screen a power supply for a monitor has to be able to synchronize its switching frequency to an external signal, typically the monitor’s horizontal sync flyback signal. Such a sync technique cannot be used in colour TVs, however, since, unlike monitors, a colour TV’s horizontal deflection frequency is too low. Since, unlike monitors, a colour TV’s horizontal deflection frequency is too low. Instead, an SMPS for a colour TV makes use of the so called quasi resonant technique. In this technique a capacitor is added between the MOSFET drain and source, which lowers both the rising slope of the voltage Vds between the MOSFET’s drain and source and the falling slope of the reverse voltage across the secondary side rectifier diodes when the MOSFET turns off. The shallower slopes reduce the dV/dt switching noise and switching loss, because the MOSFET turns on when Vds is at a minimum or zero.

5. Conclusion

In this paper, the digital control techniques for power quality improvement have been discussed and also the modelling of a digitally controlled switching power supply system using is presented. Simulation and experimental results add to the merits of the paper. Also FPGA module for PWM generator is presented with its advantages. From the research point of view all the main contributions to digital solutions for SMPS demonstrate control approaches with minimum hardware resources and reduced complexity. Feasibility of completely integrated digital controllers was demonstrated. Testing of TV power supply is done by power quality analyser and its result is added. The techniques presented in the paper are considered to be better alternatives to power quality improvement, because of reduced size of filters in power supplies, higher efficiency, lower cost and enhanced reliability. The authors of the paper deals that the techniques presented beneficial to designers, users, manufacturers and research engineers dealing with power quality improvement research. Digital power techniques have been proposed for some years now, but have not been able to successfully compete with analog solutions. Thanks to increase in IC density, hard work on the part
of semiconductor suppliers and a mature and reliable CMOS technology, digital processing for power conversion applications now is very attractive.

References


Paresh J. Shah was born in India in 1967. He received the B.E. degree in Industrial Electronics Engineering from Amravati University, Maharashtra in 1989. He has completed M.E. degree in Power Electronics from SGSITS, Indore in 1997, with Distinction. He is also pursuing Ph. D. from SGSITS, Indore, Madhya Pradesh. He has published 6 papers in international conferences and 16 papers in national conferences. At present he is working as Associate Professor in E&TC department at SSBT’s COET Jalgaon, Maharashtra. He has also received Shiksha Ratan Puraskar on 08/09/10. His special field of interest is Power Electronics, Power Quality and VLSI design.